Novel Flip-Chip Bonding Technology for *W*-Band Interconnections Using Alternate Lead-Free Solder Bumps

Kiyomitsu Onodera, Takao Ishii, Shinji Aoyama, Suehiro Sugitani, and Masami Tokumitsu

***Abstract*—A novel lead-free flip-chip technology for mounting high-speed compound semiconductor ICs, which have a relatively severe limitation regarding high-heat treatment, is presented. Solder bump interconnections of 0.95Sn–0.05Au were successfully fabricated by reflowing multilayer metal film at as low a temperature as 220 °C. The bumps were designed to have a diameter of 36 μm with a gap between the chip and the motherboard of 24 μm. The electrical characteristics of flip-chip-mounted coplanar waveguide chips were measured. The deterioration in reflection loss in the flip chip mounting was less than 3 dB for frequencies up to *W*-band.**

***Index Terms*—Flip-chip devices, microassembly, lumped element microwave circuits.**

I. Introduction

LATELY, the quality of chip interconnections greatly affects the performance of entire optical communication subsystems containing high bit rate integrated circuits (ICs). The inherently high characteristic impedance of widely used thermosonic wire bonding causes drastic performance degradation at high frequencies. Extremely short wires, only a few hundred micrometers long, are needed for frequencies in the W band. [1]. Flip-chip interconnection is emerging as a leading technology that can meet the high-frequency requirements [2]. The most popular and successful flip-chip technology has been the lead–tin solder bump interconnection introduced by IBM in the early 1960s [3]. The advantages of solder bumps are low interconnection parasitic inductance, a relatively low-temperature process, and fine positioning and height accuracy due to the self-alignment of melted solder [4], [5]. However, the increasing awareness of lead's danger to the environment and public health stimulated substantial research and development of lead-free solder alloys. We have developed an alternate lead-free solder-bump and process technology for flip-chip mounting of high-speed compound semiconductor ICs, which have a relatively severe limitation regarding high-heat treatment. This letter describes the fabrication and electrical performance of enhanced flip-chip interconnections, which are suitable for applications at frequencies up to W band.

Manuscript received March 22, 2002; revised May 7, 2002. The review of this letter was arranged by Associate Editor Dr. Arvind Sharma.

The authors are with NTT Photonics Laboratories, NTT Corporation, Kanagawa, Japan (e-mail: onodera@aecl.ntt.co.jp).

Digital Object Identifier 10.1109/LMWC.2002.804555.

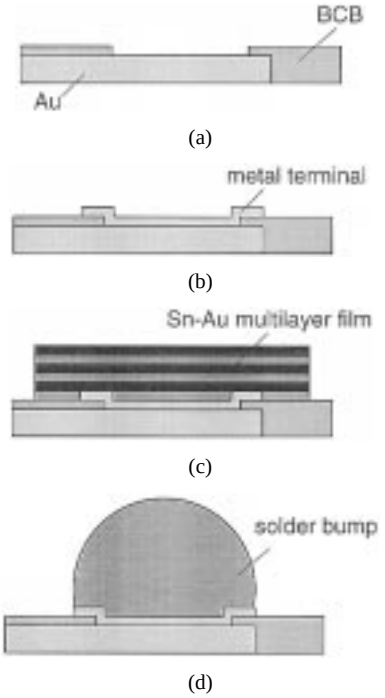

Fig. 1. Process for making lead-free solder bumps: (a) via holes are scraped using O_2/CF_4 RIE on the edge of waveguides; (b) wettable metal terminals composed of Ti/Pt/Au are placed on via holes; (c) multilayer film of tin and gold is sequentially deposited and lifted off; (d) precursors are heated to 220 °C for 2 min with a resin flux coating.

II. Microbump Fabrication

We surveyed several lead-free solder alloys, examining whether they can be 1) evaporated without multiple electron beams or 2) reflowed at temperatures lower than 250 °C [6]. However, most of them could not be evaporated using one electron beam, because of enormous difference between the vapor pressures of the constituent metals, and did not exhibit interdiffusion at their eutectic temperature. The Au–Sn alloy we selected is a rare material that exhibits interdiffusion. The multiple layers by sequential deposition can be homogenized at its eutectic temperature. In fact, the system also has a quite low eutectic temperature of 217 °C at 0.95Sn–0.05Au, which is low enough to apply it to GaAs- or InP-based devices.

The fabrication procedure is shown in Fig. 1. The base metal, Ti (100 nm)/Pt (500 nm)/Au (15 000 nm), which forms waveguides, is deposited on GaAs substrate and coated by 1.8–μm benzocyclobutene (BCB). The via holes on which

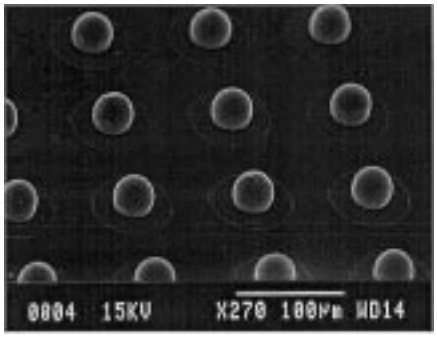

Fig. 2. Microphotograph of 0.95 Sn–0.05 Au solder bumps after reflowing.

the microbumps are to be laid are formed by O_2/CF_4 reactive ion etching (RIE) of the edge of the waveguides [Fig. 1(a)]. The wettable metal terminals, composed of Ti (100 nm)/Pt (100 nm)/Au (100 nm), are placed on the via holes [Fig. 1(b)]. The diameter of the metal terminals is 36 μm. To make the microbump precursors using the lift-off process, footprints are formed on the metal terminals by applying a 15-μm-thick photoresist. The diameter of the footprints is 80 μm. A multilayer film of tin and gold is sequentially deposited by electron beam evaporation. The cycles of sequential deposition are ten, and the thickness of each tin and gold film is 600 nm and 20 nm, respectively [Fig. 1(c)]. The total film thickness is 6.2 μm. The estimated compositional ratio of the alloy metals is $Sn:Au = 0.946:0.054$ (mole%). After lift-off, the precursors are heated to 220 °C for two min with a resin flux coating [Fig. 1(d)]. Fig. 2 shows a SEM photograph of the microbumps after reflowing. They have a remarkably good uniformity because the volume of the bump metal depends only on the high-precision lithography and the evaporated metal thickness. The alloy composition can also be precisely controlled by the thickness of each metal.

III. Measurement Results

To evaluate a frequency characteristic of the solder-bumped interconnects, a chip with a coplanar waveguide (CPW) and a motherboard with coplanar stubs were designed and fabricated on GaAs substrate. The configuration is shown in Fig. 3(a) and (b). The CPW of the chip was formed on GaAs/BCB (1.8 μm). The chip is 2 × 1 mm and the CPW length is 1.6 mm, where the slot width and the spacing are 25 and 40 μm, respectively. Meanwhile, the coplanar stubs of the motherboard were formed directly on GaAs substrate, where the slot width and the spacing were 55 and 75 μm, respectively, which is equivalent to the geometry of the pad on ICs.

The GaAs chip was flip-chip mounted on the GaAs motherboard as shown in Fig. 3(c). The total length of CPW straddling the chip and motherboard was 2.4 mm. The flip-chip samples were examined closely under an infrared microscope from the top, and the bump height was estimated to be 24 μm with high uniformity, which agreed with numerical calculations. Bump shape theoretically depends on surface tension and the difference in pressure between inside and outside the melted solder. However, bump height can be mainly determined by the volume of solder and the diameter of the wettable terminal

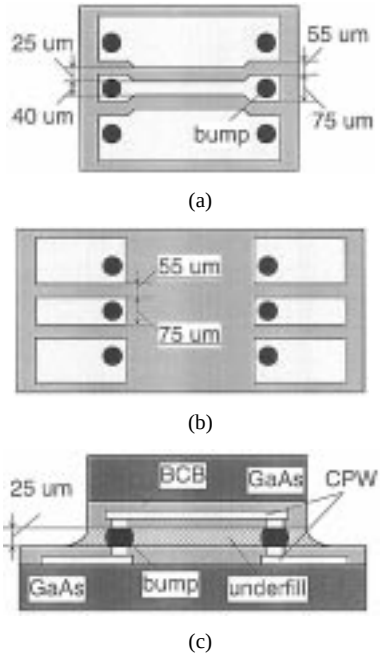

Fig. 3. Schematic views of (a) coplanar waveguides on chip (b) coplanar slots on motherboard and (c) flip-chip mounted sample.

metal. Bonding pressure fluctuation has little influence on the bump shape. Therefore, the solder-bump height, in addition to their high positioning accuracy, can be accurately defined and reproducibly controlled. After the flip-chip mounting, an underfill based on an epoxy resin with permittivity of 3.8 at 1 kHz was inserted between the chip and motherboard for reinforcement of the connection. The cure conditions were 125 °C for 30 min and 165 °C for 2 h.

The electrical performance of the flip-chip mounted sample was measured by means of an on-wafer probe using a HP8510B network analyzer at a frequency range from 100 MHz to 110 GHz. Fig. 4 shows the measured reflection and insertion loss of the sample against frequency. The solid and broken lines indicate the results with and without an underfill, respectively. The results for 2-mm-long CPW on GaAs/BCB (1.8 μm) is shown as a gray line. The flip-chip bonding using these lead-free bumps provides excellent performance up to the W band. The insertion and reflection loss with (without) an underfill are 0.8 dB/mm (0.8 dB/mm) at 110 GHz and 6 dB (9 dB) under dc to 110 GHz, respectively. The results for the CPW only are an insertion loss of 0.6 dB/mm and a reflection loss of under 9 dB. The reflection deterioration was less than 3 dB in the flip-chip mounting.

To ascertain the cause of somewhat poor reflection of the CPW at *W*-band frequencies, the characteristic impedance of CPW was calculated from the S-parameters measured in different length, 0.5, 1.0, and 2.0 mm. The frequency dispersion of impedance of 0.2 Ω/GHz was extracted on assumption of linear dependence against frequency. The impedance increased to 70 Ω at 100 GHz, which would accounted for deteriorated reflection in the CPW. Meanwhile, the effective permittivity of the CPW was calculated to be 5.6 using an electromagnetic analysis, whereas that with a 25-μm-thick underfill above the CPW was 6.8. The characteristic impedance of the CPW decreases

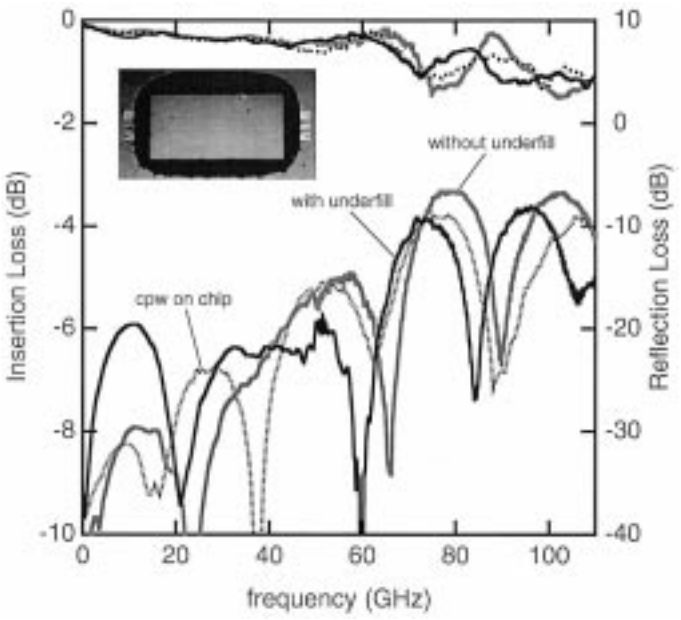

Fig. 4. Measured electrical characteristics of flip-chip mounted sample. Inset is photograph showing sample from top.

10% owing to the underfill. In our sample, the motherboard surface below the chip was not metallized and the bump height was 24 μm. The characteristic impedance therefore hardly changed from that when it was not flip-chipped. The deviation is within 2–3% [7]. Therefore, 10% decrease of impedance made the reflection with an underfill a little better than that without an underfill in Fig. 4.

IV. Summary

A novel flip-chip technology for high-speed compound semiconductor ICs operating at up to *W*-band frequencies has been presented. The lead-free 0.95Sn–0.05Au microbump interconnections, made from multilayer metal film, can be fabricated at a temperature as low as 220 °C. The deterioration in reflection loss in the flip chip mounting compared with only a CPW line was less than 3 dB. This flip-chip bonding technology using alternate lead-free solder bumps should be applicable up to *W*-band frequencies.

Acknowledgment

The authors thank Dr. M. Muraguchi and Dr. H. Toba for their continuous encouragement. They are also grateful to Dr. T. Akeyoshi and J. Aaratake for assistance in fabrication and fruitful discussions.

References

[1] T. Krems, W. Haydl, M. Massler, and J. Rudiger, "Millimeter-wave performance of chip interconnections using wire bonding and flip chip," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1995, pp. 247–250.

[2] W. Heinrich, A. Jentzen, and H. Richer, "Flip-chip interconnects for frequencies up to W band," *Electron. Lett.*, vol. 37, no. 3, pp. 180–181, 2001.

[3] J. H. Lau, *Flip Chip Technologies*: McGraw-Hill, 1995, ch. New York.

[4] H. Tsunetsugu, T. Hayashi, K. Katsura, M. Hosoya, N. Sato, and N. Kukutsu, "Accurate, stable, high-speed interconnections using 20–30-μm-diameter microsolder bumps," *IEEE Trans. Comp., Packag., Manufact. Technol. A*, vol. 20, no. 1, pp. 76–82, 1997.

[5] H. Tsunetsugu, T. Hayashi, M. Hosoya, K. Katsura, M. Hirano, and Y. Imai, "Flip chip bonding technique using transferred microsolder bumps," *IEEE Trans. Comp., Packag., Manufact. Technol. C*, vol. 20, no. 4, pp. 327–334, 1997.

[6] T. Ishii, S. Aoyama, and M. Tokumitsu, "Fabrication of 0.95Sn0.05Au solder micro-bumps for flip-chip bonding," *J. Electron. Mater.*, vol. 30, no. 6, pp. L25–27, 2001.

[7] W. Heinrich, A. Jentzen, and G. Baumann, "Microwave characteristics of flip-chip interconnections for multi-chip modules," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1998, pp. 1083–1086.